WHAT IS CLAIMED IS:

1. An auxiliary device for operating both an M-DOC series flash memory and a non-X86 system processor in synchronism, comprising:

a first logic circuit enabled by a first address line of the non-X86 system processor for changing output thereof from a first level to a second level;

a delay circuit for delaying the second level output of the first logic circuit a predetermined period of time prior to clearing the first logic circuit for changing output thereof from a second level to a first level; and

a second logic circuit for performing a logical operation on the output of the first logic circuit and a CS pin of the non-X86 system processor prior to coupling to a CS pin of the M-DOC series flash memory.

2. The auxiliary device as claimed in claim 1, wherein the delay circuit comprises a plurality flip-flops (FFs).

3. The auxiliary device as claimed in claim 2, wherein each of the FFs is positive edge trigger.

4. The auxiliary device as claimed in claim 2, wherein each of the FFs is a D-FF.

5. The auxiliary device as claimed in claim 1, wherein the delay circuit is a D-FF.

6. The auxiliary device as claimed in claim 1, wherein the second logic circuit is a logical OR gate.